REMARKS/ARGUMENTS

Claims 25-35 are amended, and claims 36-53 are newly added. Claims 25-53 are now pending in the application. Applicants request reexamination and reconsideration of the application in light of the following remarks.

Claims 25-35 were rejected under 35 USC 102(e) as anticipated by US Patent No. 6,701,474 to Cooke et al. ("Cooke"). Applicants respectfully traverse this rejection.

Before discussing the rejection, it may be helpful to provide some background information regarding semiconductor testing. The dies of a semiconductor wafer are tested by writing test signals to the dies and reading response data from the dies. Typically, a tester generates the test signals and evaluates the response data. A probe card provides the interface to and from the dies and must be custom designed for both the tester and the dies.

A typical probe card includes tester contacts for making electrical connections with signal channels from the tester. The probe card also include probes for contacting the pads of the dies. Signal paths through the probe card connect the tester contacts and probes. As mentioned, the probe card must be custom designed for the tester and the dies. For example, the tester contacts must be custom oriented to interface with the tester and the probes must be custom positioned to contact the die pads. Moreover, the tester contacts must be connected to the proper probes. For example, if the dies are memory dies, tester contacts that receive address signals from the tester must be connected to probes that contact address input pads on the dies. The routing of signals through the probe card must also meet timing and other design requirements. For example, if the die is a memory die, the routing of the address signals through the probe card must be such that all of the address signals arrive at the probes (and thus the die address pads) at the same time or within a specified delay tolerance. As another example, the integrity of signals as they pass through the probe card must be maintained (e.g., a logic high signal must not lose strength as it passes through the probe card and thereby improperly change to a logic low signal).

Before a probe card is used to test the dies of a semiconductor wafer, the probe card must be designed, verified, and manufactured. If the probe card design is incorrect, dies may fail testing not because the dies are defective but because the probe card is defective. Thus, the design, verification, and manufacture of a probe card must take place before the probe card can be used to test dies.

A fundamental difference between the claims of the instant application and Cooke is as follows: the claims of the instant application are directed to a process of designing and verifying the probe card. In contrast, Cooke is concerned with processes for designing and verifying the die (referred to as an "IC" in Cooke), including creating patterns of test signals for testing the die. Of course Cooke mentions use of a probe card, because probe cards are used to test dies. But other than briefly mentioning the well known fact that a probe card must be custom designed for the die (see Cooke column 12, lines 20-23), Cooke does not describe any process for designing or verifying the design of a probe card.

Indeed, many of the sections of Cooke relied on in the Office Action describe testing the IC, which as discussed above, cannot occur until after the probe card is designed, verified, and manufactured. Thus, much of Cooke simply cannot be applicable to the claims of the instant application.

Turning now to the claims of the instant application, independent claim 25 recites a method of making a probe card in which the information needed to design the probe card (i.e., information describing the semiconductor wafer to be tested) is communicated over a network (e.g., the Internet) from the customer to the probe card manufacturer. The probe card manufacturer then generates a proposed design for the probe card. The network (e.g., the Internet) is used for further communications with the customer regarding the acceptability of the proposed design of the probe card.

There are several advantages to using a network as recited in claim 25. As just one example, the use of a network facilitates communications with customers located long distances and across many time zones (e.g., overseas) from the manufacturer. The customer may, for example, log onto the network during its business hours and post information describing the wafer to be tested. Later, during the business hours of the manufacturer, the manufacturer can log onto the network and receive the wafer information, generate the design, log back onto the network and post the design. Still later, during the customer's business hours, the customer can log onto the network, check the design, and post desired changes. As an example of another advantage, because the system is networked based, the manufacture's network computer may be configured to generate automatically a probe card design in response to the manufacturer's wafer information and then post the design for the customer to access via the network. Many other advantages and variations are possible.

As discussed above, although Cooke mentions that a probe card must be custom designed for the IC to be tested, Cooke does not describe a process for designing the probe card. Not surprisingly, therefore, Cooke does not disclose using a network to communicate information necessary to design a probe card. Figures 1-4 and associated text and columns 8, 10, 11, and 12 are describe processes for designing the IC—not the probe card. Again, the mere mention of the well known fact that all probe cards must be custom designed for the ICs they test is not a disclosure of a process for designing the probe cards much less a disclosure of a process for designing probe cards that includes use of a network for communicating information between customer and probe card manufacturer. Therefore, Cooke does not anticipate independent claim 25.

Moreover, dependent claims 26-35 recite additional features of the invention that Cooke likewise fails to disclose.

For example, claim 26 recites that a graphical user interface is provided to the customer through which the information necessary to design the probe card is entered. Column 5, lines 1-8 of Cooke describe the interface that the probe card provides for routing test signals and response data to and from the IC while testing the IC. That is not a graphical interface through which a customer enters data describing an IC for use in designing a probe card. Columns 11 and 12 of Cooke, which describe a process of designing an IC and creating test signal patterns for testing the IC, likewise does not disclose the graphical user interface recited in claim 26. Claim 26 thus further distinguishes over Cooke.

As another example, claim 27 states that the graphical user interface of claim 26 is a Web page. Nowhere in column 8 does Cooke disclose using a Web page to enter information used to design a probe card. As yet another example, claim 29 recites "verifying said proposed probe card design." The text associated with Figures 4 and 5 and columns 11 and 12 of Cooke discuss verifying the IC design but never mention verifying the design of the probe card. Claim 30 recites drawings depicting the probe card. Figures 6 and 7 of Cooke illustrate the creation of patterns of test signals to be written to the IC; Figures 6 and 7 have nothing to do with drawings depicting a probe card. Claim 31 recites notifying the customer of proposed changes to the design of a yet-to-be-manufactured probe card. (The probe card of claim 31 necessarily has not yet been manufactured because its design is not finalized but, per the express language of claim 31, is still being changed.) In contrast, columns 17 and 18 discuss the use of an already-

manufactured probe card to test an IC. Nowhere in columns 17 and 18 is there any discussion regarding modifying a proposed design of a yet-to-be-manufactured probe card. Claim 32 recites simulating the proposed design of the probe card. In contrast, at column 1, lines 13-34, Cooke discusses simulation of the IC design—not the probe card design.

For all of the foregoing reasons, dependent claims 26-35 further distinguish over Cooke.

New independent claim 36 is also directed to a method of designing a probe card—not an IC as disclosed in Cooke. Independent claim 36 and its dependent claims (claims 37-44) therefore distinguish over Cooke.

New independent claim 45 is directed to a method of verifying a probe card design. As discussed above, Cooke discloses nothing concerning the verification of a probe card. Independent claim 45 and its dependent claims (claims 46-53) thus distinguish over Cooke.

As a final note, an Information Disclosure Statement (IDS) was filed in November 2004 and is listed on PAIR as having been received by the PTO on November 22, 2004. Applicants request that the prior art filed with that IDS be considered and the listing of prior art be initialed and returned to Applicants.

In view of the foregoing, Applicants submit that all of the claims are allowable and the application is in condition for allowance. If the Examiner believes that a discussion with Applicants' attorney would be helpful, the Examiner is invited to contact the undersigned at (801) 323-5934.

Respectfully submitted,

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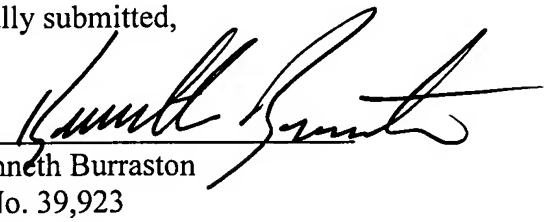
By 
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